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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,256	12/27/2000	Howard H. Chen	YO999-153DIV	4783

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/748,256	Applicant(s) CHEN ET AL.	
	Examiner ori nadav	Art Unit 2811	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-39 and 41-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-39 and 41-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 29-36, 41-42 and 45-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun (5,399,507).

Regarding claims 29, 36, 41, 45 and 46, Sun teaches in figure 4 and related text a hybrid semiconductor device comprising a bulk silicon region 11 comprising single crystal silicon (column 2, lines 61-62) and an SOI region comprising an insulator layer 18 formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least two isolation oxides 22, 24 formed in an upper portion of the single crystal silicon so as to form a plurality of islands of the single crystal silicon on an upper surface of the insulator layer, wherein a sidewall of the insulator layer 23 is angled so that a width of the upper surface of the insulator layer is larger than a width of a lower surface of the insulator layer, wherein at least one isolation oxide comprises a first isolation oxide 24 formed adjacent to a first end portion of the insulator layer, a third isolation oxide 22 formed adjacent

to a middle portion of the insulator layer, and wherein the first isolation oxide extends laterally beyond the first end portion.

Sun does not teach a second isolation oxide formed adjacent to a second end portion of the insulator layer wherein the second isolation oxide extends laterally beyond the second end portion.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a second isolation oxide formed adjacent to a second end portion of the insulator layer wherein the second isolation oxide extends laterally beyond the second end portion in Sun's device in order to form the device as taught by Sun by providing protection to the thin film active area also at the second end portion of the device. The combination is motivated by the teachings of Sun who points out the dual function of the isolation oxide which is formed adjacent to an end portion of the insulator layer (column 3, lines 34-38).

Regarding claims 34 and 42, Sun teaches in figure 4 and related text isolation oxides and insulator layer formed of the same material, wherein the insulator layer is formed only in an SOI region and not in a bulk silicon region of the substrate.

Regarding claim 35, Sun teaches in figure 4 an upper surface of the isolation oxides and the single crystal silicon are planarized.

Regarding claim 36, the single crystal silicon over the insulator layer has the same crystal orientation and structure as that in the bulk silicon region, because it is the same single crystal silicon layer.

Regarding claims 32, 33, 47, 48 and 30, 49, 52, Sun teaches substantially the entire claimed structure, as applied to claims 29 and 46 above, except forming a crystallized silicon layer by depositing and annealing the amorphous silicon, and horizontally growing the single crystal silicon having the same crystal orientation as the insulator layer by using the lower portion of the silicon as a seed, using isolation oxides to remove defects on the SOI region and forming isolation oxides by forming trenches and depositing oxide in the trenches.
Forming a crystallized silicon layer by depositing and annealing the amorphous silicon, and horizontally growing the single crystal silicon having the same crystal orientation as the insulator layer by using the lower portion of the silicon as a seed, using isolation oxides to remove defects on the SOI region and forming isolation oxides by forming trenches and depositing oxide in the trenches, as recited in claims 32, 33, 47, 48 and 30, 49, are processing limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 31, 50 and 53-54, Sun does not teach an insulator layer having a thickness in the range of 1000A to 5000A and 2000A to 10,000A, an upper portion of the single crystal silicon layer having a thickness in the range of 500A to 3000A, and an angle between a bottom surface of the insulator layer and a sidewall of the insulator layer is about 103 degrees. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulator layer having a thickness in the range of 1000A to 5000A and 2000A to 10,000A, an upper portion of the single crystal silicon layer having a thickness in the range of 500A to 3000A, and an angle between a bottom surface of the insulator layer and a sidewall of the insulator layer is about 103 degrees in Sun's device, because it is well within the skills of an artisan to optimize the performance of the device by adjusting the angle between a bottom surface of the insulator layer and a sidewall of the insulator layer, and forming the insulator layer and the silicon layer at the required thickness.

Regarding claim 55, the device of Sun comprises a plurality of islands wholly formed on the insulator layer.

Regarding claim 56, Sun does not teach in figure 4 and related text that at least one island comprises of a defective region. Therefore, in absence of evidence to the contrary, it is held the Sun's device comprises at least one island being substantially devoid of a defective region, as claimed.

2. Claims 37-39 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun in view of Tanaka (Jp 10-303385).

Regarding claims 37-39 and 43-44, Sun teaches substantially the entire claimed structure, as applied to claims 29, 41 and 42 above, except forming a DRAM memory device on the silicon bulk and a MOSFET logic device on the SOI region.

Tanaka teaches in figure 1f a DRAM memory device 11 on the silicon bulk and a MOSFET logic device 13 on the SOI region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a DRAM memory device on the silicon bulk and a MOSFET logic device on the SOI region, as taught by Tanaka, in Sun's device in order to provide a hybrid device wherein the DRAM can operate at high speed with less power consumption and the logic circuits are adequately isolated.

Respons to Argum nts

3. Applicant's arguments with respect to claims 29-39 and 41-57 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference A is cited as being related to an SOI structure comprises islands.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may b submitted to T chnology center (TC) 2800 by facsimil transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
November 4, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800